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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/879,208	OOWAKI ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/21/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *14-29,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *14-29,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt is acknowledged of paper submitted under 35 U.S.C. 1 19(a)-(d), claiming priority from Japanese Patent Application No. 182899 filed on June 29, 1998 which papers have been placed of record in the file.

Request for Continued Examination Application (RCE)

The request filed on 09/ 21/2005 which was entered and forwarded to the examiner on 09/29/2005 for a Continued Examination Application (RCE) under 37 CFR 1.114 (d) based on parent Application No. 09/302165 is acceptable and a RCE has been established. An action on the RCE follows.

Information Disclosure Statement

No further IDS has been submitted by the Applicants' after the one submitted on December 14, 2001.

Preliminary Amendment Status

Acknowledgment is made of entry of preliminary amendment filed July 22, 2005.

Therefore claims 14, 18, 22-24 and 27-29, 31-32 as amended by the amendment and claims 15-17,19-21 and 25-26 as previously recited are currently pending in the Application.

Claims 1-13, 30 and 33-39 have been cancelled.

Claim Objections

Claim 18 line 5 instead of reciting " selectively forming a first film on said semiconductor substrate" which can be recited as " forming a first film on a

portion of said semiconductor substrate" .

It is confusing and not clear if Applicants' are referring to selectively forming by means of different processes (the specification as originally filed only supports a single process having several embodiments) different conditions or selectively forming first film on the whole semiconductor substrate but not on other parts of the device or selectively forming i.e. forming the first film on a portion (selective with respect to the entire substrate) of the substrate. In view of various possibilities the claim is not clear.

The same objection was also stated in the previous Office Action , Applicants' response though a bona fide attempt , does not over come the objection and therefore failure to receive a proper response will result in a FINAL objection.

Further the first film should be identified as " first oxide film". This requirement was previously made to make claim 18 consumarate with Applicants' arguments wherein they stated that their invention was allegedly distinguished over prior because their invention is drawn to first oxide film.

Therefore in keeping with current U.S. practice , either applicants' recite the limitation in the claims on which they are trying to distinguish their invention i.e. " first oxide film" or if applicants' do not want to recite the limitation then as their claims are not presently reciting the limitation, it (the limitation) cannot form the basis of distinguishing the present claims from the applied prior art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 14-29 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (U.S. Patent No. 5,270,257, herein after Shin) and further in view of Wen (U.S. Patent No. 5,949,116 herein after Wen) . (for response to Applicants' arguments see section below).

With respect to claim 14 Shin describes a method for producing a MIS transistor comprising a semiconductor substrate, impurity diffusion regions formed on the substrate serving as source/drain regions, and a gate electrode provided above a channel region between the source/drain regions, said method comprising : (Shin fig. 3a-c,) selectively forming a first film on said semiconductor substrate,(Shin fig. 3 c-e#22- nitride) etching said semiconductor substrate to form a first groove by using said first film as a mask, (Shin figure 3 a) forming a second film in said first groove and thereafter removing said first film; (Shin figure 3a-c) diffusing an impurity onto a surface of said semiconductor substrate using said second film as a mask (Shin 3a-c) . Shin does not specifically disclose the steps of forming an impurity diffusion region including a pad of a bottom of the first groove (i.e. an impurity diffusion region) diffusing an impurity onto a surface of said semiconductor substrate using said second film as a mask to form the impurity diffusion regions including a part thereof extending below the first groove ; forming an insulator film on said impurity diffusion regions and

thereafter removing said second film to form a second groove in the semiconductor substrate.

Shin does not specifcally describe the steps of forming an impurity diffusion region .

However, Wen , a patent from the same filed of endeavor , describes in figures length devices (figs. 2A to B) length devices including the steps of forming an impurity diffusion region . (figs. 2A to B an d col. 2 lines 21-52, col.2 lines 44-46) to provide a process for fabricating a Mos device that allows a contact widow elsewhere than source/drain region thus resulting in smaller device .

Therefore it would have been obvious to one of ordinary skill in the art , at the time of the invention to include Wen's step of forming an impurity diffusion region including a part of a bottom of the first groove to form self-aligned source/drain regions in small channel length devices in Shin's method , the motivation to make the above combination is to provide a process for fabricating a Mos device that allows a contact widow elsewhere than source/drain region thus resulting in smaller device . (Wen col. 1 lines 49 to57).

The remaining limitations of claim 14 are :

and thereafter removing the second film to form a second groove on the semiconductor

substrate (Figure 2C removal of 201 ,207) so that a top surface of the impurity diffusion region of the semiconductor substrate is higher than a bottom surface of the second groove, (figure 2C 200 above 209) forming a gate insulator film in said second groove

and controlling a thickness of the gate insulator film so that the top surface of each of said gate insulator film is higher than a top surface of said impurity diffusion region' (interpreted to mean " and" instead of with" -see 1 12 objection above) and forming a gate electrode on the top surface of said gate insulator film. (Wen figure 2 D to F, gate insulator film (2 1 0) .

With respect to claim 15, Shin describes wherein the second film is semiconductor film (Shin film 24 is poly silicon , Shin col. 4 line 41) and forming a sacrificial film in the first groove before forming the second film in the first groove (Wen figs. 2 B and C) removing the sacrificial film after removing the second film to form the second groove. (Wen fig. 2B # 207and Figure 2C).

With respect to claim 16, Shin describes wherein a step of polishing a surface of the second film by using the first film as a stopper (Shin fig. 1 1 , col. 6 lines 66-67).

With respect to claim 17,Shin describes forming a protective film in the second groove before forming the gate insulator film in the second groove (Shin fig. 14 # 285).

With respect to claim 18, Shin describes it repeats all the steps of claim 14 (see above) and further includes the step of : polishing the gate insulator film by using the insulator as a stopper (Shin fig. 1 1, col. 6 lines 66-67).

Claims 19-21 repeat the steps of claims 15-17 and are rejected for reasons set forth above.

Claim 22 repeats the steps of claim 18 except for the absence of the second film-forming step and is rejected for reasons stated under claim 18 above.

Claims 23 wherein the source/ drain regions are elevated by an epitaxial growth technique before the diffusion step. (Shin fig. 3 e # 28a and b, col. 4 lines 65-critical. In re Woodruff 919 F.ZD. 1575, 1578, 16 USPQ 2d 1934, 1936 (Fed. Cir. 1990).

Claims 25-26 repeat the steps of claims 19 and 21 above and are rejected for reasons stated above.

With respect to claim 27, repeats the steps of claims 18 and 22 and is rejected for reasons set out above.

Claims 28-31 repeat the steps of claims 23, 24, 25 and 26 and are rejected for reasons set out above.

B. Claims 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shin (U.S. Patent No. 5,270,257, herein after Shin) previously applied in view of Wen (U.S. Patent No. 5,949,1 16, hereinafter Wen) as applied to claims 14-31 above and further in view of Lee (U.S patent No. 6,248,622, hereinafter Lee).

With respect to claim 32 , in addition to the steps of claims 18 and 22, claim 32 further recites the source/drain regions forming an inclined surface between the top surface of the semiconductor layers and the channel region (Shin fig. 3e # 26a and b) , forming a dummy film on the channel region that borders the semiconductor layers (part of 24 etched away).

Depositing a gate electrode on a top side of the gate insulator film to form a gate electrode having a cross section of a T shape.

Wen describes the forming of a gate electrode on a top side of the gate insulator film to form a gate electrode . (Wen figs. 2f and3).

Shin and Wen do not specifically describe the gate having a cross section of a T-shape .

However, Lee, a patent from the same filed of endeavor, describes in fig. 3 B-D and col. 5 lines 7-8 describes a metal layer and a damascene structure that has a T-shaped cross-section to form a circuit/device with improved speed and avoiding logical cross-talk errors.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Lee's interconnect having a T-shaped cross section in Krivokapic method to form a circuit/device with improved speed and avoiding logical cross-talk errors. (Lee col. 1 lines 41-44).

Response to Arguments

Applicant's arguments filed on July 22, 2005 with respect to claims 14-29, 31-32 have been considered but not persuasive for the following reasons :

Applicants' are engaging in piece meal analysis of individual references applied whereas the rejection is based on the combine teachings of the applied Shin and Wen references and for claim 32 Shin, Wen and Additional Lee references.

Applicants' first contention states that the applied Wen reference does not teach a gate insulator film and then add Wen's element 211 is an insulating layer , therefore

giving Applicants' claims the broadest reasonable interpretation for gate insulator film , Wen's element 210 is a gate insulating film isolating conductive element 211 from gate. Similar to that described in at least Applicants' figures 6A to 6C and 6D to E.

It is noted that above Applicants' argument are not consumarate in scope with the presently recited claims because present claims do not exclude Wen's teachings. If Applicants' want to maintain their contention that there claims should be limited as restricted in their argument then Applicants' may amend the claims to include "forming a gate insulator film that is a part of the gate structure only " so as to possible distinguish over Wen on the basis of this argument.

Similarly, Applicants' second contention that Wen's element 210 is formed " outside of the region beneath the gate is not consumarate with the presently recited claims which does not require the gate insulator film to be formed beneath the gate only

Further , Applicants' arguments that Wen's element 210 and 211 are not between the source and drain regions is directly contrary to Applicants' argument/ contention that Wen's element 210 and 211 form the source /drian and if this is true then element 210 is between source and drain as these form a periferal regions see figures of the regions alleged to be source and drain by the Applicants'.

Therefore it is not the Examiner who has mischaracterized Wen , but rather the Applicants' while reciting the claims broadly are arguing limitation that are not presently recited in the claims.

Therefore each and every limitation of the presently recited independent claims 14 and 18 have been clearly shown to be taught by the combined teachings of Shin and Wen ,

Dependent claims 15-17 and 19-21 were alleged to be allowable because of their dependency on allegedly allowable claims 14 and 18, but as seen above claims 14 and 18 are not allowable claims 15-17 and 19-21 are also not allowable.

Applicants' contention that Shin does not teach/ suggest its gate insulator film 23 has a top surface higher than a top surface of the impurity diffusion region is not persuasive because Applicants;' are considering the Shin's full disclosure which includes figure 3e which shows film 23 above low concentration n –type source/drain regions 26 a and b (col. 4 lines 63-66, etc.).

Therefore claims 22 and 23-27 are rejected.

Similar arguments were made w.r.t claim 27 as made with claim 23 above and therefore claim 27 is also rejected.

Therefore all pending claims are rejected.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fahmy Wael can be reached on (571) 272-1714. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven H. Rao

Patent Examiner

December 06, 2005.

HOWARD WEISS
PRIMARY EXAMINER